REMARKS

The Office Action mailed November 10, 2004 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Subject Matter Indicated Allowed or Allowable

Applicants gratefully acknowledge the indication of allowance of Claims 19 – 24, 26 – 30, 32, and 35. It is presumed that since these are all dependent claims, their allowance is contingent upon incorporation thereinto of the subject matter of the independent base claims and intervening claims.

Applicants are further grateful for the indication of allowability of Claims 38 – 39, 41 – 44, 47 – 48, and 50 – 52, subject to their re-writing in independent form including the subject matter of the base and intervening claims.

For the reasons outlined below, Applicants urge that these base claims and intervening claims are allowable on their merit, and respectfully decline the incorporation of their subject matter into the claims indicated allowable.

Claim Objections

The objection to Claims 31, 33 and 34 is unclear because these claims do refer to the other claims in the alternative, as evidenced the word "or." Withdrawal of the objection is respectfully urged.

Rejection(s) Under 35 U.S.C. § 112, First Paragraph

Claim 25 was rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is mostly nearly connected, to make and/or use the invention. Claim 25 has been amended to remove the offending matter. Such removal, it will be appreciated, does not narrow the scope of the claim.

Rejection(s) Under 35 U.S.C. § 102 (b)

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as anticipated by Brilman et al. (U.S. pat. no. 4,663,631). Claim 1 reads as follows:

> 1. A phase detector and signal locking system controller comprising:
>
> a first phase detector receiving at least a first input source and a second input source and outputting at least a first control signal;
>
> a second phase detector receiving at least the first input source and the second input source and outputting at least a second control signal; and
>
> a control unit receiving at least the first control signal, the second control signal, a first gain factor, and a second gain factor and outputting at least a phase measurement result signal.

Brilman et al. fails to disclose *inter alia* "a control unit receiving at least the first control signal, the second control signal, a first gain factor, and a second gain factor and outputting at least a phase measurement result signal."

According to the Office Action, timing unit 3 of Brilman et al. corresponds to the controller of Claim 1, and, like said controller, receives from phase detectors 9 and 15 outputs

PLL-x and PLL-y, respectively. Furthermore, it is alleged, timing unit 3 receives first (AGC-x) and second (AGC-y) gain factors and outputs a phase measurement resultant signal.

Applicants respectfully disagree. Timing unit 3 actually serves to control the operation of the system of Brilman et al. by *providing* timing signals for its various components. Thus, rather than *receive* signals from these components, timing unit 3 *provides* operating signals and parameters. This role is evident from FIG. 1 and the associated discussion. FIG. 1 shows arrows corresponding to PLL-x, PLL-y, AGC-x and AGC-y emanating from timing unit 3. Corresponding labels are provided at switches 24, 25, 32 and 33 consistent with conventional labeling techniques indicating that these outputs from timing unit 3 are provided to the switches to control their states. The vertical arrows depicted at each switch are simply part of the manner in which switches are conventionally illustrated in technical and engineering drawings. The discussion in Brilman et al. fully supports this contention. For example, with respect to switch 24, Brilman et al. explains that the switch "closes in time interval T$\sum$y *on the reception of* a control signal PLL-y from the timing unit 3." (Col. 4, ll. 21 – 22, emphasis added). With respect to switch 25, Brilman et al. explains that the switch "closes in time interval T$\sum$x *on the reception of* a control signal PLL-x from timing unit." (Col. 4, ll. 23 – 25, emphasis added).

It will be appreciated that, according to the M.P.E.P., a claim is anticipated under 35 U.S.C. § 102(b) only if each and every claim element is found, either expressly or inherently described, in a single prior art reference.[1] The aforementioned reasons clearly indicate the contrary, and withdrawal of the 35 U.S.C. § 102(b) rejection based on Brilman et al. is respectfully urged.

Claim 2 depends from Claim 1 and is allowable for at least the same reasons.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 3 – 7, 10 – 14 and 17 – 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Brilman et al. in view of Dosho et al. (2002/0007436).

Claim 3 reads as follows:

> 3. A phase detector and signal locking system controller comprising:
>
> a first phase detector receiving at least a first input source and a second input source and outputting at least a first phase indicator signal and a second phase indicator signal;
>
> a second phase detector receiving at least the first input source and the second input source and outputting at least an order indicator signal;
>
> a synchronizing circuit receiving at least the first phase indicator signal, the second phase indicator signal, and a system clock signal and outputting at least a first synchronized phase indicator signal and a second synchronized phase indicator signal; and
>
> a post processing and control unit receiving at least the first synchronized phase indicator signal, the second synchronized phase indicator signal, the order indicator signal and the first input source and outputting a phase measurement result signal.

Neither Brilman et al. nor Dosho et al. teach the last limitation of Claim 3, namely:

> a post processing and control unit receiving at least the first synchronized phase indicator signal, the second synchronized phase indicator signal, the order indicator signal and the first input source and outputting a phase measurement result signal.

The Office Action fails to address this deficiency. Further, Dosho et al. does not disclose a synchronizing circuit as described and claimed in Claim 3, with the circuit receiving first and

[1] Manual of Patent Examining Procedure (MPEP) § 2131. See also *Verdegaal Bros. v. Union Oil Co. of California,*

second phase indicator signals from first and second phase detectors (Dosho et al. only discloses a single phase detector, 40) and a system clock signal, and outputting at least a first synchronized phase indicator signal and a second synchronized phase indicator signal. Thus to allege generally that Claim 3 would be obvious based on a combination of Brilman et al. and Dosho et al. would not only be grounded in impermissible hindsight, but would any case fail to meet or render obvious all of the limitations of Claim 3.

As the Examiner will note, according to the Manual of Patent Examining Procedure (M.P.E.P.),

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.[2]

Based on the above discussion, it will be appreciated that the Office Action failed to establish a *prima facie* case of obviousness. The obviousness rejection of Claim 3 (and 4 – 7, 10 – 14 and 17 – 18 dependent therefrom) based on the combination of Brilman et al. and Dosho et al. is improper and should be withdrawn.

Claims 3 – 7, 10 – 14 and 17 – 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Brilman et al. in view of Dosho et al., and further in view of DuFour (U.S. pat. no. 6,229,864).

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814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[2] M.P.E.P § 2143.

The above shortcomings of the combination of Brilman et al. and Dosho et al. are not remedied by DuFour. Withdrawal of the obviousness rejection based on these references is respectfully urged.

Conclusion

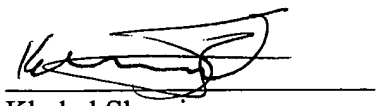
In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fee, including those necessary to obtain extensions of time to render timely the filing of the instant Reply, or credit any overpayment not otherwise paid or credited, to our deposit account No. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.

Dated: 2/10/05



Khaled Shami
Reg. No. 38,745

Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640
Tel. (408) 282-1855
Fax. (408) 287-8040